

D4SO2G64xG(I)-p18

16GB DDR4 Unbuffered SO-DIMM based on 8Gb, x8, Dual rank
RoHS Compliant Product

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Overview

This chapter gives an overview of the 16GB DDR4 Unbuffered SO-DIMM and describes its main characteristics.

Features

- 260-Pin Unbuffered Small Outline Dual-In-Line Memory Module
- Capacity: 16GB
- JEDEC-Standard
- SPD Power Supply: $V_{DDSPD} = 2.5$ or 3.3 V
- Power Supply: $V_{DD}, V_{DDQ} = 1.2 \pm 0.06$ V
- DRAM Activating Power Supply: $V_{PP} = 2.5$ V (2.375 V – 2.75 V)
- Bi-directional Differential Data-Strobe
- 64 Bit Data Bus Width without ECC
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1 (Clock)
- On-Die Termination (ODT)
- ZQ Calibration supported
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- Low Power Auto Self Refresh Mode is supported
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- Serial Presence Detect (SPD) EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.18inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
D4SO2G64xGz-p18qqS	16GB	2Gx64	2	DDR4 Unbuffered SO-DIMM

Notes:

- x: Speed Grade (refer Table 2)
- z: Temperature Grade (refer Table 3)
- p: PCB version (refer Table 4)
- qq: DRAM brand (refer Table 5)
- s: DRAM Die version (refer Table 5)

Table 2 - Speed Grade

Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)	Supported CAS Latency
6	DDR4-2666	1333MHz (0.750ns@CL19)	10,11,12,13,14,15,16,17,18,19,20
4	DDR4-2400	1200MHz (0.833ns@CL17)	10,11,12,13,14,15,16,17,18
1	DDR4-2133	1067MHz (0.938ns@CL15)	9,11,12,13,14,15,16
8	DDR4-1866	933MHz (1.071ns@CL13)	9,11,12,13,14

Table 3 - Temperature Grade

Part Number	Temperature Grade	T _{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85°C < T_{case} ≤ 95°C.

Table 4 - PCB Version

Part Number
Alphabetical character from A

Table 5 - Memory Chip Information – 16GB

Part Number	Base Device Brand	Base Device	Type	Die Version
D4SO2G64xGz-p58HA	Hynix	H5AN8G8NAFR	1Gx8	A
D4SO2G64xGz-p58HM	Hynix	H5AN8G8NMFR	1Gx8	M
D4SO2G64xGz-p58NC	Nanya	NT5AD1024M8C3	1Gx8	C
D4SO2G64xGz-p58NA	Nanya	NT5AD1024M8A3	1Gx8	A
D4SO2G64xGz-p58SD	Samsung	K4A8G085WD	1Gx8	D
D4SO2G64xGz-p58SC	Samsung	K4A8G085WC	1Gx8	C
D4SO2G64xGz-p58SB	Samsung	K4A8G085WB	1Gx8	B

Table 6 – Addressing

Parameter	16GB
Refresh count	8K
Device bank group address	4 BG[1:0]
Row address	64K A[15:0]
Device bank address per group	4 BA[1:0]
Column address	1K A[9:0]
Device configuration	8Gb (1Gx8)
Module rank address	2 /S[1:0]
Number of devices	16

Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V _{SS}	2	V _{SS}	131	A3	132	A2
3	D5	4	D4	133	A1	134	NC
5	V _{SS}	6	V _{SS}	135	V _{DD}	136	V _{DD}
7	D1	8	D0	137	CK0	138	NC
9	V _{SS}	10	V _{SS}	139	/CK0	140	NC
11	/DQS0	12	/DM0, /DBI0	141	V _{DD}	142	V _{DD}
13	DQS0	14	V _{SS}	143	PARITY	144	A0
15	V _{SS}	16	D6	145	BA1	146	A10, AP
17	D7	18	V _{SS}	147	V _{DD}	148	V _{DD}
19	V _{SS}	20	D2	149	/CS0	150	BA0
21	D3	22	V _{SS}	151	A14, /WE	152	/RAS
23	V _{SS}	24	D12	153	V _{DD}	154	V _{DD}
25	D13	26	V _{SS}	155	ODT0	156	A15, /CAS
27	V _{SS}	28	D8	157	NC	158	A13
29	D9	30	V _{SS}	159	V _{DD}	160	V _{DD}
31	V _{SS}	32	/DQS1	161	NC	162	NC
33	/DM1, /DBI1	34	DQS1	163	V _{DD}	164	V _{REFCA}
35	V _{SS}	36	V _{SS}	165	NC	166	SA2
37	D15	38	D14	167	V _{SS}	168	V _{SS}
39	V _{SS}	40	V _{SS}	169	D37	170	D36
41	D10	42	D11	171	V _{SS}	172	V _{SS}
43	V _{SS}	44	V _{SS}	173	D33	174	D32
45	D21	46	D20	175	V _{SS}	176	V _{SS}
47	V _{SS}	48	V _{SS}	177	/DQS4	178	/DM4, /DBI4
49	D17	50	D16	179	DQS4	180	V _{SS}
51	V _{SS}	52	V _{SS}	181	V _{SS}	182	D39
53	/DQS2	54	/DM2, /DBI2	183	D38	184	V _{SS}
55	DQS2	56	V _{SS}	185	V _{SS}	186	D35
57	V _{SS}	58	D22	187	D34	188	V _{SS}
59	D23	60	V _{SS}	189	V _{SS}	190	D45
61	V _{SS}	62	D18	191	D44	192	V _{SS}
63	D19	64	V _{SS}	193	V _{SS}	194	D41
65	V _{SS}	66	D28	195	D40	196	V _{SS}
67	D29	68	V _{SS}	197	V _{SS}	198	/DQS5
69	V _{SS}	70	D24	199	/DM5, /DBI5	200	DQS5
71	D25	72	V _{SS}	201	V _{SS}	202	V _{SS}
73	V _{SS}	74	/DQS3	203	D46	204	D47
75	/DM3, /DBI3	76	DQS3	205	V _{SS}	206	V _{SS}
77	V _{SS}	78	V _{SS}	207	D42	208	D43

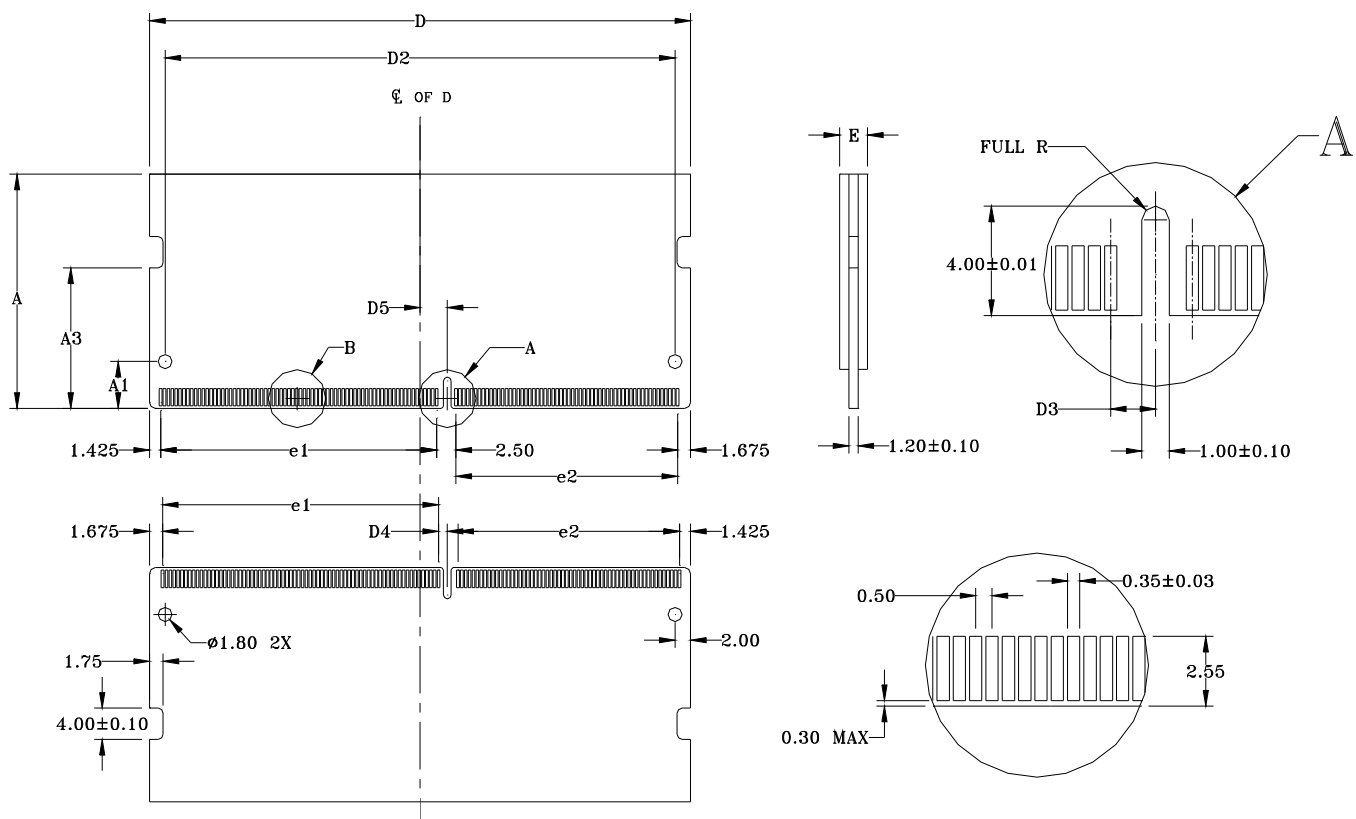
Pin	Name	Pin	Name	Pin	Name	Pin	Name
79	D30	80	D31	209	V _{SS}	210	V _{SS}
81	V _{SS}	82	V _{SS}	211	D52	212	D53
83	D26	84	D27	213	V _{SS}	214	V _{SS}
85	V _{SS}	86	V _{SS}	215	D49	216	D48
87	NC	88	NC	217	V _{SS}	218	V _{SS}
89	V _{SS}	90	V _{SS}	219	/DQS6	220	/DM6, /DBI6
91	NC	92	NC	221	DQS6	222	V _{SS}
93	V _{SS}	94	V _{SS}	223	V _{SS}	224	D54
95	NC	96	NC	225	D55	226	V _{SS}
97	NC	98	V _{SS}	227	V _{SS}	228	D50
99	V _{SS}	100	NC	229	D51	230	V _{SS}
101	NC	102	V _{SS}	231	V _{SS}	232	D60
103	V _{SS}	104	NC	233	D61	234	V _{SS}
105	NC	106	V _{SS}	235	V _{SS}	236	D57
107	V _{SS}	108	/RESET	237	D56	238	V _{SS}
109	CKE0	110	NC	239	V _{SS}	240	/DQS7
111	V _{DD}	112	V _{DD}	241	/DM7, /DBI7	242	DQS7
113	BG1	114	/ACT	243	V _{SS}	244	V _{SS}
115	BG0	116	/ALERT	245	D62	246	D63
117	V _{DD}	118	V _{DD}	247	V _{SS}	248	V _{SS}
119	A12	120	A11	249	D58	250	D59
121	A9	122	A7	251	V _{SS}	252	V _{SS}
123	V _{DD}	124	V _{DD}	253	SCL	254	SDA
125	A8	126	A5	255	V _{DDSPD}	256	SA0
127	A6	128	A4	257	V _{PP}	258	V _{TT}
129	V _{DD}	130	V _{DD}	259	V _{PP}	260	SA1

Pin Description

Pin Name	Description	Pin Name	Description
V _{DD}	SDRAM I/O & core power supply	V _{PP}	SDRAM activating power supply
V _{REFCA}	SDRAM command/address reference supply	V _{SS}	Power supply return (ground)
A0-A15	SDRAM address bus	BA0-BA1	SDRAM bank select
BG0-BG1	SDRAM bank group select	CKE0	SDRAM clock enable lines
ODT0-ODT1	SDRAM on-die termination control lines	/WE	SDRAM write enable
/CAS	SDRAM column address strobe	/RAS	SDRAM row address strobe
/CS0	Rank select lines	/ACT	SDRAM activate
CK0	SDRAM clocks (positive line of differential pair)	/CK0	SDRAM clocks (negative line of differential pair)
D0-D63	DIMM memory data bus	/DM0-/DM7, /DBI0-/DBI7	SDRAM data masks/data bus inversion
DQS0-DQS7	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS7	SDRAM data strobes (negative line of differential pair)
PARITY	SDRAM parity input	SCL	EEPROM bus clock
SDA	EEPROM data line	SA0-SA2	SDRAM address input
/ALERT	SDRAM /ALERT	/RESET	Set SDRAMs to a known state
V _{TT}	SDRAM I/O termination supply	NC	Spare pins (no connect)
V _{DDSPD}	EEPROM positive power supply	-	-

Module Dimension

Figure 1 – 260 Pin DDR4 Unbuffered SO-DIMM



Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1	6.00 Basic		
A3	17.85	18.00	18.15
D	69.45	69.60	69.75
D2	65.60 Basic		
D3	1.375 Basic		
D4	1.125 Basic		
D5	3.50 Basic		
e1	35.50 Basic		
e2	28.50 Basic		
E			3.70

Notes:

- 1 All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- 2 Tolerance on all dimensions ± 0.15 unless otherwise specified.
- 3 All dimensions are in millimeters.

Revision History

Revision	Descriptions	Release Date
1.0	First release	Dec, 2015
2.0	Update the Memory Chip Information in Table 5	Jul, 2016
3.0	Add "VDDSPD voltage: 2.5V or 3.3V" into Features	Sep, 2016
4.0	Update the Memory Chip Information in Table 5	Jul, 2017
5.0	Update the Memory Chip Information in Table 5	Jul, 2017
6.0	- Update the Memory Chip Information in Table 5 - Add DDR4-2666 speed grade	Aug, 2018
7.0	Update the Memory Chip Information in Table 5	Apr, 2019
8.0	- Update the Memory Chip Information in Table 5 - Update Global Presence	Mar, 2021

MEMPHIS | Global Presence

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